IN THE SPECIFICATION:

Please amend the specification as follows:

Please amend the paragraph on page 11, from lines 4 through 8, as follows:

FIG. 4(A) –FIG. 4(C) are ~~FIG. 4 is a~~ waveform charts ~~chart~~ illustrating the response of detection voltage Vsns to output level instruction signal Vramp in the feedback control system of the high frequency power amplification circuit in the embodiments of the present invention and in the prior invention.

Please amend the paragraph on page 12, from lines 10 through 12, as follows:

FIG. 8(A) is a graph showing the frequency characteristic of the gain of the closed loop in the control system in the second embodiment.

Please amend the paragraph bridging pages 20 and 21, from line 19 on page 20 through line 6 on page 21, as follows:

It is generally said that when the phase margin of a loop is not more than 45°, the stability of oscillation cannot be ensured. However, application of the first embodiment improves the phase margin of open loop in the feedback control system of the high frequency power amplification circuit using the square root conversion circuit 30, illustrated in FIG. 1. Thus, the stability of oscillation can be ensured. As the result, the following advantage is produced: even if the output level instruction signal Vramp abruptly changes, as illustrated in (A) of FIG. 4, the detection signal Vsns fed back to the inverting input terminal of the error amplifier 50 does not develop ringing as ~~unlike in~~ (C) of FIG. 4. Thus, the response of loop to output level instruction signal Vramp is enhanced.

Please amend the paragraphs on pages 35 and 36, from line 16 on page 35 through line 21 on page 36, as follows:

The radio communication system in FIG. 11 comprises a high frequency module (hereafter, referred to as "RF module") 100; a module for high frequency power amplifier (hereafter, referred to as "power module") 200; a baseband circuit 300; a front end module 400; and a microprocessor (CPU) 500. The RF module 100 is formed by mounting on one ceramic substrate a high frequency signal processing circuit (high frequency IC) 110 constituted as a semiconductor integrated circuit having a modulation-demodulation circuit

capable of GMSK modulation and demodulation in the GSM and DCS systems; a band pass filter SAW 120a,120b comprising an elastic surface-wave filter which removes unwanted waves from reception signals; a low noise amplifier LNA 130a,130b which amplifies reception signals; and the like. The power module 200 includes [[a]] high frequency power amplification circuits (power amplifiers) 210a,210b [[10]] which drive an antenna ANT as load to carry out transmission; an output power control circuit 230; and the like. The microprocessor (CPU) 500 is a controller which controls the entire system.

The baseband circuit 300 is provided with a baseband processing function for generating I- and Q-signals based on transmission data (baseband signal) and processing I- and Q-signals extracted from reception signals. The baseband circuit 300 is constituted as a semiconductor integrated circuit. Hereafter, this is referred to as "baseband IC." The front end module 400 contains filters LPF 410a,410b which suppress noise ~~noises~~, such as harmonics, contained in transmission signals outputted from the RF power module 200; transmission/reception changeover switches 420a and 420b; a dividing filter 430; and the like. The microprocessor (CPU) 500 generates control signals for the high frequency IC 110 and the baseband IC 300 and output level instruction signals Vramp for the power module 200.

Please amend the paragraph on page 39, from lines 4 through 24, as follows:

Up to this point, the invention made by the inventors has been described based on the embodiments. However, the present invention is not limited to the above embodiments, and may be modified in various ways to the extent that its scope [[cope]] is not departed from, needless to add. Some examples are as follows ~~will be taken~~. In the above embodiments, the square root conversion circuit 30 is provided between the current detection circuit 20 and the current-voltage conversion circuit 40. Instead of the square root conversion circuit 30, an nth root conversion circuit (n is an integer not less than 2) or a logarithmic conversion circuit may be provided. Instead of provision of an nth root conversion circuit or a logarithmic conversion circuit, the following constitution may be adopted: the current detection circuit 20 or the current-voltage conversion circuit 40 is provided with such a characteristic that its output is nth root-functionally or logarithmic-functionally changed relative to its input. In the high frequency power amplification circuit in the above embodiments, the power amplifying FETs are connected in three stages. However, [[such]] a constitution may be adopted whereby [[that]] they are connected in two stages or four or more stages ~~may be adopted~~.